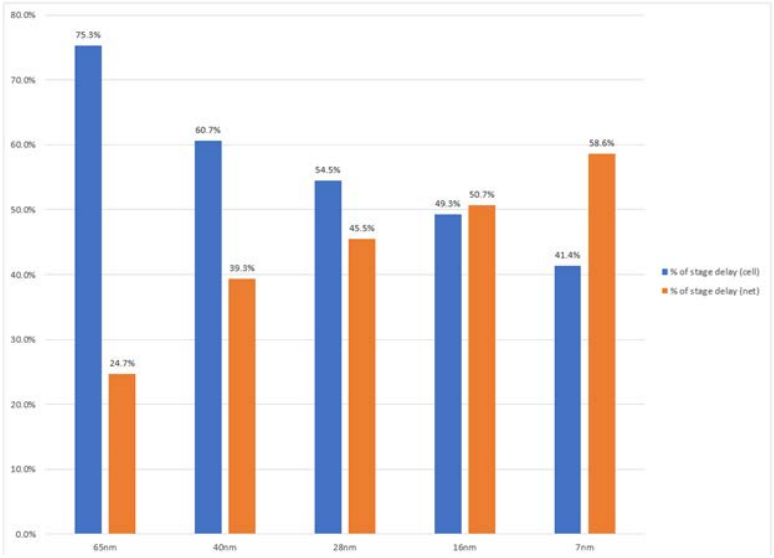
A Place-and-Route Paradigm Shift: Detailed-Route-Centric Solution Now Required

Each technology node adds tougher physical design challenges and more stringent design rules. Modern lithography requires dual patterning and layer coloring. High currents through narrow wires risk electro-migration failures. The routes have a high impact on all these issues. As a result, it is much harder to route dense designs.

Meanwhile, one of the biggest hurdles remains timing closure, and that, too, heavily depends on the router.

Wire RC delay is a larger component of stage delay at smaller process nodes



As wire widths shrink faster than standard cells, routes in cutting edge technologies become longer and narrower. Design rules make it difficult to insert redundant vias. Wire and via resistance now impact the transition waveform shape, even on short and medium length routes. Higher cross-coupling capacitance and net resistance simultaneously impact timing through larger crosstalk effects. As a result, wire delay takes an increasing percentage of cycle time. By 7nm, for nets of significant length, wire delay is measured as more than half of total stage delay. As a result, critical paths are much harder to close.

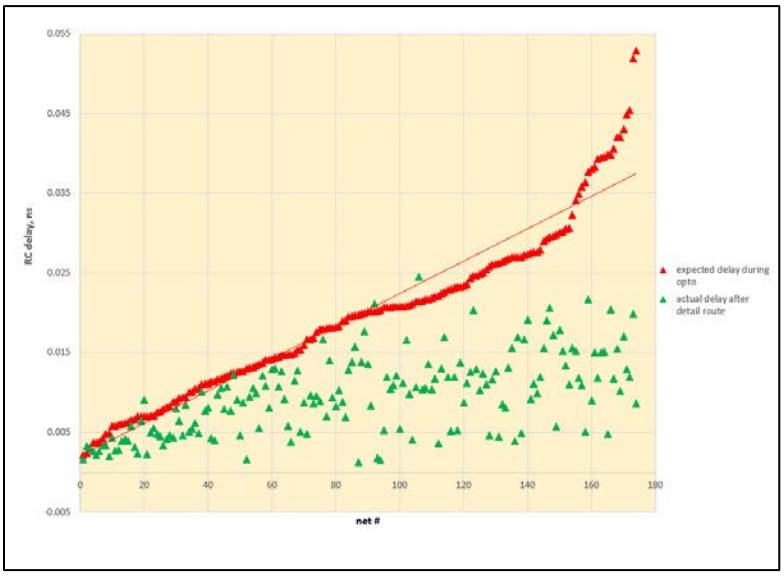
Placement-based estimates for wire RC delays are no longer adequate

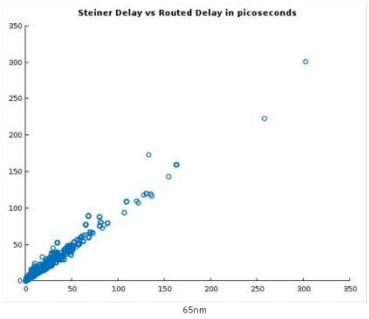
For 40nm and 28nm designs, timing closure could be achieved through good cell placement as routing had less impact. But as the industry moves from 16nm down to 7nm and beyond, it is increasingly difficult to close timing through placement alone. There are too many router-related considerations to guarantee that pre-route Steiner wire estimates can be achieved by the final detailed routing pattern.

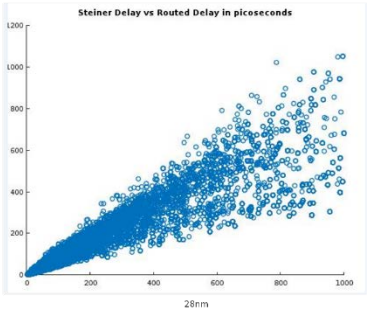
Depending on the layers a router chooses for any given route, resistance on that route can be seen to vary by upwards of 500%.

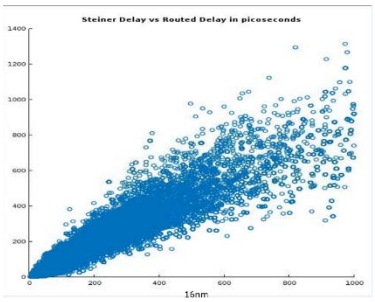
This translates into RC delay estimates that can vary as much as 300%. Similarly, the effects of crosstalk delay cannot be reasonably estimated unless layer information is well understood.

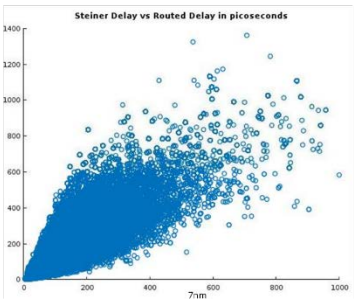
The figure on the right illustrates, for a 7nm design, how much a net's RC delay can vary if it is routed on different layers.











Most place-and-route systems attempt to estimate post-route delays through global routing or heuristic shortcuts. Using the global router during optimization can cause unacceptable runtimes for large designs.

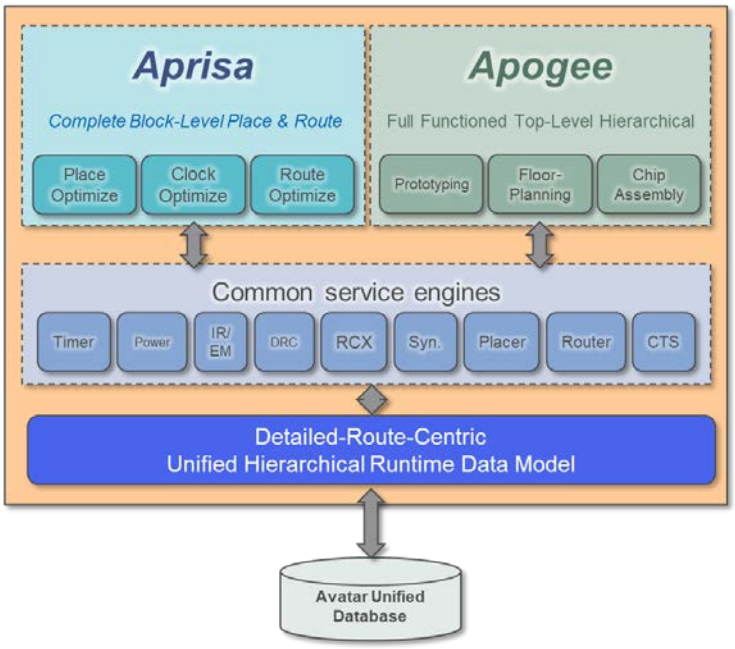
Heuristic shortcuts attempt to reduce this runtime but trade off accuracy. In addition, often a different routing engine is used for global and detailed routing, making the estimates even more inaccurate.

This means that optimizations performed before detailed routing must be repeated once real detailed routing info is available. This reduces predictability, increases iterations, increases power consumption due to overdesign, and reduces the feasibility of closing timing on difficult designs.

As illustrated on the left, the timing inaccuracies from pre- to post-route get worse as the technology shrinks from 65nm to 28nm to 16nm down to 7nm processes.

A new paradigm is called for

Route effects must be considered earlier in the flow, that is, during placement. For this reason, we need to move from a placement-centric tool where route effects are estimated to a router-centric solution. Avatar Integrated Systems' Aprisa place-and-route software has been re-architected to address these design challenges. At every stage of the physical design, Aprisa takes into consideration all deep submicron routing issues, such as timing closure, pin access, dual pattern coloring, signal noise, electro-migration. Every step of the flow is aware of, and can react to the effects of routing on the design. This allows for less timing variability, easier routability, and faster design closure.



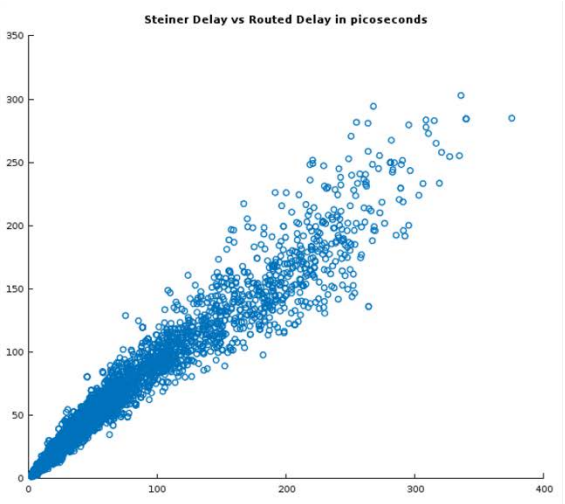
We do this in three key ways:

- Aprisa's Unified Data Model (UDM) is the single database architecture for placement, optimization, routing, and analysis. All Aprisa engines utilize the same data models, objects, and attributes in real time. Nothing gets lost in translation between flow steps.
- The Common Service Engine (CSE) enables analysis engines and optimization engines to work in concert. Every implementation engine can make dynamic real-time calls to analysis engines at will. Optimizations are made with accurate data the first time. Extraction and timing data gets updated dynamically and seamlessly.
- The Route Service Engine (RSE) provides proper routing information on a per-net basis to any engine within the system that needs it. Minimizing "Total Net Delay" for the design is key to the Aprisa route-centric system. Placement and optimization assign non-default route rules to nets in the course of managing congestion and timing closure. The RSE manages the route topology during all phases of optimization and reports to the calling optimization engine the net routing topology, such as metal layers used, RC parasitics and crosstalk delta delay. Only by predicting and guiding the route topology early in the design can optimization be performed effectively and efficiently.

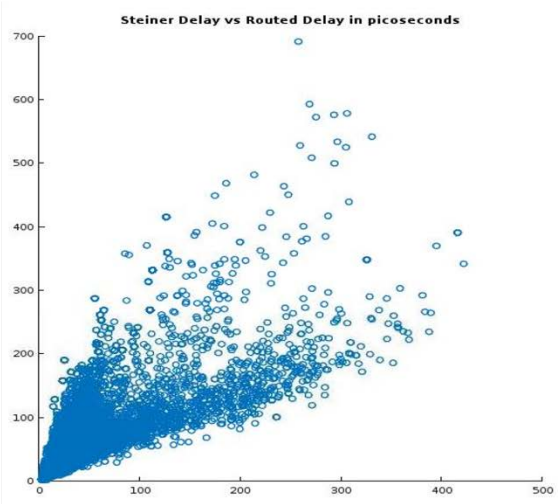
RSE engine at work on critical nets

The figures below shows the RSE engine at work on critical nets. The scatter plot on the left shows nets detailed-routed versus Steiner-routed net delay with RSE active. These nets have routing properties that have been automatically assigned at the placement and optimization phase and are carried through the detailed routing optimization phase, giving accurate timing throughout the entire flow. The scatter plot on the right shows the same set of nets routed without RSE active. These nets do not have routing properties assigned. Note that the correlation between Steiner net delay and routed net delay for RSE-routed nets is very tight, while correlation without RSE is much looser.

Route-centric



Not route-centric



Being able to anticipate and design for routing issues early in the flow is critical, but equally critical is being able to implement the routed design. The RSE offers the smartest, most powerful detailed router in the industry to address modern routing challenges. It has been optimized to address the high resistivity of advanced process nodes. In addition to accurately implementing the pre-route net topology, there are numerous built-in features which will boost designer productivity. For example, Aprisa is the only router aware of dual pattern layer coloring up front, inherently avoiding odd cycle violations. Signal electro-migration violations are automatically detected and resolved.

The router can not only enable speedy design closure, it can also achieve higher design utilization at 7nm, shrinking die sizes and minimizing design cost. The route-centric physical design paradigm is the reality of modern physical design. Avatar Integrated Systems' Aprisa place-and-route software has been designed explicitly to address this new paradigm.

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